

Code: EC6T1

**III B.Tech - II Semester – Regular/Supplementary Examinations
AUGUST 2021**

**VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

- a) Define propagation delay of a CMOS inverter.
- b) Define body bias effect.
- c) Define any two layout design rules.
- d) Give expression for propagation delay of an inverter.
- e) What is constant electric field scaling?
- f) Write short notes on transmission gate.
- g) What is semicustom design?
- h) Short notes on standard cell-based PLD?
- i) What is the need for testing?
- j) What is the principle behind logic verification?
- k) What is latch-up? How to prevent latch-up?

PART – B

Answer any *THREE* questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the V-I characteristics. 8 M
- b) Explain the DC transfer characteristics of a CMOS Inverter with necessary conditions for the three different regions of operation. 8 M
3. a) Derive an expression for the rise time, fall time, and propagation delay of a CMOS inverter. 8 M
- b) Discuss in detail with a neat layout, the design rules for a CMOS inverter. 8 M
4. a) Derive the scaling factors of MOS device. 8 M
- b) Discuss the limitation of interconnects and contact resistance scaling. 8 M
5. a) Implement full subtractor using PLA and PAL. 8 M
- b) Draw and explain the Xilinx FPGA architecture. 8 M

6. a) Explain the principle of Built-In Self-Test (BIST). What are the advantages and disadvantages of BIST? 8 M
- b) Explain what is meant by a Stuck-at-1 fault and a Stuck-at-0 fault with suitable example. 8 M